

Amendments to the Specification:

Please replace the paragraph beginning on page 25 with the following amended paragraph:

In FIG. 9, 2 divider 110 also includes a first inverting multiplexer 345A and a second inverting multiplexer 345B. The select input of inverting multiplexer 345A (345B) is coupled to RESET2, a first input of the inverting multiplexer is coupled to ground (VCC) and a second input of the inverting multiplexer is coupled to CLKINB (CLKIN). When RESET2 is high, the output of inverting multiplexer 345A is high (VCC) and the output of inverting multiplexer 345B is low (ground). When RESET2 is low, the output of inverting multiplexer 345A (345B) is inverted CLKINB (inverted CLKIN). The output of inverting multiplexer 345A is coupled to the gate of PFETs T16 and T19 and an NFET T25 (node P22). The output of inverting multiplexer 345B is coupled to the gate of NFETs T21 and T18 and a PFET T26 (node P23). The drain of PFET T26 and the source of NFET T25 are coupled to node P21. The source of PFET T26 and the drain of NFET T25 are coupled together to form a node P24 hence forming a transmission gate. The gates of PFETs T15 and T20 and NFETs T17 and T22 are coupled to node P24. The 2 divider 110 is completed by a pull down NFET [T25] T25, the drain of NFET T27 coupled to node P21, the source of NFET T27 coupled to ground, and the gate of NFET T27 coupled to RESET2. When RESET 2 is high, NFET T27 is on and node P21 is pulled low. With node P21 low, CLKOUT2 is high and no division occurs.

Please replace the paragraph beginning on page 26 with the following amended paragraph:

In operation, when RESET2 is high, node P21 transitions to 0, node P22 transitions to 1 and node P23 transitions to 0, PFETs T16 and T20 and NFETs T18 and T22 are off, nodes P18 and P19 hang, NFET T25 and PFET T26 are on and P21=P24=0. When RESET2 transitions to 0 and if CLKIN=1 and CLKINB=0 then node P22=1, node P23=0, PFETs T16 and T20 and NFETs T18 and T22 are off, nodes P18 and P19 hang, nodes P18 and P19 hang, NFET T25 and PFET T26 are on and P21=P24=0. The 2 divider 110 is essentially a divide by 2 state machine four states which transition in the following order.